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| Patent Number: | 7003746 | | | |
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| Petition Issued Date: | May 18,2010 | | | |
| Title of Invention: | METHOD AND APPARATUS FOR ACCELERATING THE VERIFICATION OF APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGNS | | | |
| First Named Inventor/Applicant Name: | Stanley M. Hyduke | | | |
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| Petition automatically granted by EFS | Hyduke_4507P3174_Pett.pdf | 842026 | no | 3 | |
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| 2 Fee Worksheet (PTO-875) | fee-info.pdf | 32178 | no | 2 | |
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